Low-Power Bidirectional I²C Isolators

Check for Samples: ISO1540, ISO1541

FEATURES

- **Isolated Bidirectional, I²C Compatible, Communications**
- **Supports up to 1 MHz Operation**
- **3-V to 5.5-V Supply Range**
- **Open Drain Outputs with 3.5-mA Side 1 and 35-mA Side 2 Sink Current Capability**
- **-40°C to 125°C Operating Temperature**
- **±50 kV/μs Transient Immunity (Typical)**
- **HBM ESD Protection of 4 kV on All Pins; 8 kV on Bus Pins**

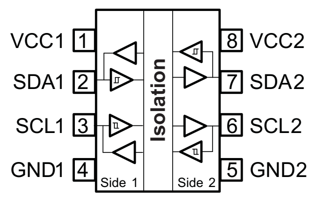
APPLICATIONS

- **Isolated I²C Bus**
- **SMBus and PMBus Interfaces**
- **Open-drain Networks**
- **Motor Control Systems**
- **Battery Management**
- **I²C Level Shifting**

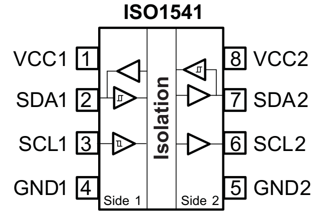
SAFETY AND REGULATORY APPROVALS

- **4000-V_{PK} Isolation per DIN EN 60747-5-2 (VDE 0884 Part 2) (Pending)**
- **2500-V_{RMS} Isolation for 1 minute per UL 1577 (Approved)**
- **CSA Component Acceptance Notice 5A (Pending)**
- **IEC 60950-1 and IEC 61010-1 End Equipment Standards (Pending)**

ISO1540



ISO1541



DESCRIPTION

The ISO1540 and ISO1541 are low-power, bidirectional isolators that are compatible with I2C interfaces. These devices have their logic input and output buffers separated by TI's Capacitive Isolation technology using a silicon dioxide (SiO2) barrier. When used in conjunction with isolated power supplies, these devices block high voltages, isolate grounds, and prevent noise currents from entering the local ground and interfering with or damaging sensitive circuitry.

This isolation technology provides for function, performance, size, and power consumption advantages when compared to opto-couplers. The ISO1540 and ISO1541 enable a complete isolated I²C interface to be implemented within a small form factor.

The ISO1540 has two isolated bidirectional channels for clock and data lines while the ISO1541 has a bidirectional data and a unidirectional clock channel. The ISO1541 is useful in applications that have a single Master while the ISO1540 is ideally fit for multi-master applications.

Isolated bidirectional communications is accomplished within these devices by offsetting the Side 1 Low-Level Output Voltage to a value greater than the Side 1 High-Level Input Voltage thus preventing an internal logic latch that otherwise would occur with standard digital isolators.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

PIN FUNCTIONS

ISO1540 and ISO1541	I / O	DESCRIPTION			
NAME	PIN	ISO1540	ISO1541	ISO1540	ISO1541
VCC1	1	-	-	Supply Voltage, Side 1	Supply Voltage, Side 1
SDA1	2	I / O	I / O	Serial Data, Side 1 Input/Output	Serial Data, Side 1 Input/Output
SCL1	3	I / O	I	Serial Clock Input/Output, Side 1	Serial Clock Input, Side 1
GND1	4	-	-	Ground, Side 1	Ground, Side 1
GND2	5	-	-	Ground, Side 2	Ground, Side 2
SCL2	6	I / O	O	Serial Clock Input/Output, Side 2	Serial Clock Output, Side 2
SDA2	7	I / O	I / O	Serial Data Input/Output, Side 2	Serial Data Input/Output, Side 2
VCC2	8	-	-	Supply Voltage, Side 2	Supply Voltage, Side 2

AVAILABLE OPTIONS

PRODUCT	RATED ISOLATION	PACKAGE	CHANNEL DIRECTION	MARKED AS	ORDERING NUMBER
ISO1540	4000-V_{PK} and 2500-V_{RMS} (1)	D-8	Both SDA and SCL are Bidirectional	IS1540	ISO1540D (rail)
					ISO1540DR (reel)
ISO1541			SDA is Bidirectional SCL is Unidirectional	IS1541	ISO1541D (rail)
					ISO1541DR (reel)

(1) See the Regulatory Information table for detailed Isolation specifications.

Table 1. FUNCTION TABLE (1)

POWER STATE	INPUT	OUTPUT
VCC1 or VCC2 < 2.1 V	X	Z
VCC1 and VCC2 > 2.8 V	L	L
VCC1 and VCC2 > 2.8 V	H	Z
VCC1 and VCC2 > 2.8 V	Z (2)	?

(1) H = High Level; L = Low Level; Z = High Impedance or Float; X = Irrelevant; ? = Indeterminate
(2) Invalid input condition as an I^2C system requires that a pull-up resistor to VCC is connected.

ABSOLUTE MAXIMUM RATINGS (1)(2)

				VALUES MIN	VALUES MAX	UNIT
Supply voltage	VCC1, VCC2			–0.5	6	V
Supply voltage	SDA1, SCL1			–0.5	VCC1 + 0.5	V
Supply voltage	SDA2, SCL2			–0.5	VCC2 + 0.5	V
Output current	SDA1, SCL1				±20	mA
Output current	SDA2, SCL2				±100	mA
Electrostatic Discharge	Human Body Model	ESDA, JEDEC JS-001-2012	Bus Pins		±8	kV
			All Pins		±4	
	Field-Induced-Charged Device Model	JEDEC JESD22-C101E	All Pins		±1.5	kV
	Machine Model	JEDEC JESD22-A115-A			±200	V
$T_{J(MAX)}$	Maximum junction temperature				150	°C
T_{STG}	Storage temperature range			–65	150	°C

(1) Stresses beyond those listed under ABSOLUTE MAXIMUM RATINGS cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under RECOMMENDED OPERATING CONDITIONS is not implied. Exposure to absolute-maximum-rated conditions for extended periods affects device reliability.
(2) All voltage values here within are with respect to the local ground terminal (GND1 or GND2) and are peak voltage values.

THERMAL INFORMATION

THERMAL METRIC(1)		ISO1540 ISO1541 D (8 PINS)	UNITS
θ_{JA}	Junction-to-ambient thermal resistance	114.6	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	69.6	
θ_{JB}	Junction-to-board thermal resistance	55.3	
ψ_{JT}	Junction-to-top characterization parameter	27.2	
ψ_{JB}	Junction-to-board characterization parameter	54.7	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	n/a	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
VCC1, VCC2	Supply Voltage	3		5.5	V
V_{SDA1}, V_{SCL1}	Input/Output Signal Voltages, Side 1	0		VCC1	
V_{SDA2}, V_{SCL2}	Input/Output Signal Voltages, Side 2	0		VCC2	
V_{IL1}	Low-Level Input Voltage, Side 1	0		0.5	
V_{IH1}	High-Level Input Voltage, Side 1	0.7 x VCC1		VCC1	
V_{IL2}	Low-Level Input Voltage, Side 2	0		0.3 x VCC2	
V_{IH2}	High-Level Input Voltage, Side 2	0.7 x VCC2		VCC2	
I_{OL1}	Output Current, Side 1	0.5		3.5	mA
I_{OL2}	Output Current, Side 2	0.5		35	
C_{b1}	Maximum Capacitive Load, Side 1			40	pF
C_{b2}	Maximum Capacitive Load, Side 2			400	
f_{MAX}	Maximum Operating Frequency (1)			1	MHz
T_A	Ambient Temperature	–40		125	°C
T_J	Junction Temperature	–40		136	°C
T_{SD}	Thermal Shutdown	139		171	°C

(1) This represents the maximum frequency with the maximum bus load (C_b) and the maximum current sink (I_O). If the system has less bus capacitance, then higher frequencies can be achieved.

ELECTRICAL CHARACTERISTICS

Over recommended operating conditions, unless otherwise noted

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
SUPPLY CURRENT (3V ≤ VCC1, VCC2 ≤ 3.6V)								
I_{CC1}	Supply Current, Side 1	ISO1540	V_{SDA1}, V_{SCL1} = GND1; V_{SDA2}, V_{SCL2} = GND2	See Figure 1; R_1,R_2 = Open, C_1,C_2 = Open		2.4	3.6	mA
		ISO1541				2.1	3.3	
I_{CC2}	Supply Current, Side 2	ISO1540 and ISO1541				1.7	2.7	
I_{CC1}	Supply Current, Side 1	ISO1540	V_{SDA1}, V_{SCL1} = VCC1; V_{SDA2}, V_{SCL2} = VCC2			2.5	3.8	
		ISO1541				2.3	3.6	
I_{CC2}	Supply Current, Side 2	ISO1540 and ISO1541				1.9	3.1	
SUPPLY CURRENT (4.5 V ≤ VCC1, VCC2 ≤ 5.5 V)								
I_{CC1}	Supply Current, Side 1	ISO1540	V_{SDA1}, V_{SCL1} = GND1; V_{SDA2}, V_{SCL2} = GND2	See Figure 1; R_1,R_2 = Open, C_1,C_2 = Open		3.1	4.7	mA
		ISO1541				2.8	4.4	
I_{CC2}	Supply Current, Side 2	ISO1540 and ISO1541				2.3	3.7	
I_{CC1}	Supply Current, Side 1	ISO1540	V_{SDA1}, V_{SCL1} = VCC1; V_{SDA2}, V_{SCL2} = VCC2			3.1	4.7	
		ISO1541				2.9	4.5	
I_{CC2}	Supply Current, Side 2	ISO1540 and ISO1541				2.5	4	

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SIDE 1 (Only)						
V_{ILT1}	Voltage Input Threshold "Low", Side 1 (SDA1, SCL1)		500	550	660	mV
V_{IHT1}	Voltage Input Threshold "High", Side 1 (SDA1, SCL1)		540	610	700	mV
V_{HYST1}	Voltage Input Hysteresis, Side 1 V_{IHT1}- V_{ILT1}		40	60		mV
V_{OL1} (1)	Low-Level Output Voltage, Side 1 (SDA1,SCL1)	0.5 mA ≤ (I_{SDA1} and I_{SCL1}) ≤ 3.5 mA	650		800	mV
ΔV_{OIT1} (1)(2)	Low-Level Output Voltage to High-Level Input Voltage Threshold Difference, Side 1 (SDA1, SCL1)		50			mV
SIDE 2 (Only)						
V_{ILT2}	Voltage Input Threshold "Low", Side 2 (SDA2, SCL2)		0.3 x VCC2		0.4 x VCC2	mV
V_{IHT2}	Voltage Input Threshold "High", Side 2 (SDA2, SCL2)		0.4 x VCC2		0.5 x VCC2	mV
V_{HYST2}	Voltage Input Hysteresis, Side 2 V_{IHT2} - V_{ILT2}		0.05 x VCC2			mV
V_{OL2}	Low-Level Output Voltage, Side 2 (SDA2, SCL2)	0.5 mA ≤ (I_{SDA2} and I_{SCL2}) ≤ 35 mA			400	mV
BOTH SIDES						
$\|I_I\|$	Input Leakage Currents (SDA1, SCL1, SDA2, SCL2)	V_{SDA1}, V_{SCL1} = VCC1; V_{SDA2}, V_{SCL2} = VCC2		0.01	10	µA
C_I	Input Capacitance to Local Ground (SDA1, SCL1, SDA2, SCL2)	V_I = 0.4 x sin(2E6πt) + 2.5 V		7		pF
CMTI	Common-Mode Transient Immunity	See Figure 3	25	50		kV/µs
V_{CCUV} (3)	V_{CC} Undervoltage Lockout Threshold (Side 1 and Side 2)		2.1	2.5	2.8	V

(1) This parameter does not apply to the ISO1541 SCL1 line as it is uni-directional.
(2) $\Delta V_{OIT1} = V_{OL1} – V_{IHT1}$. This represents the minimum difference between a Low-Level Output Voltage and a High-Level Input Voltage Threshold to prevent a permanent latch condition that would otherwise exist with bi-directional communication.
(3) Any V_{CC} voltages, on either side, less than the minimum will ensure device lockout. Both V_{CC} voltages above the maximum will prevent device lockout.

SWITCHING CHARACTERISTICS

Over recommended operating conditions, unless otherwise noted

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
3 V ≤ VCC1, VCC2 ≤ 3.6 V							
t_{f1}	Output Signal Fall Time (SDA1, SCL1)	See Figure 1 R_1 = 953 Ω, C_1 = 40 pF	0.7 x VCC1 to 0.3 x VCC1	8	17	29	ns
			0.9 x VCC1 to 900 mV	16	29	48	
t_{f2}	Output Signal Fall Time (SDA2, SCL2)	See Figure 1 R_2 = 95.3 Ω, C_2 = 400 pF	0.7 x VCC2 to 0.3 x VCC2	14	23	47	ns
			0.9 x VCC2 to 400 mV	35	50	100	
$t_{pLH1\text{-}2}$	Low-to-High Propagation Delay, Side 1 to Side 2	See Figure 1 R_1 = 953 Ω, R_2 = 95.3 Ω, C_1, C_2 = 10 pF	0.55 V to 0.7 x VCC2		33	65	ns
$t_{PHL1\text{-}2}$	High-to-Low Propagation Delay, Side 1 to Side 2		0.7 V to 0.4 V		90	181	ns
$PWD_{1\text{-}2}$	Pulse Width Distortion $\lvert t_{pHL1\text{-}2} - t_{pLH1\text{-}2}\rvert$				55	123	ns
$t_{PLH2\text{-}1}$ (1)	Low-to-High Propagation Delay, Side 2 to Side 1		0.4 x VCC2 to 0.7 x VCC1		47	68	ns
$t_{PHL2\text{-}1}$ (1)	High-to-Low Propagation Delay, Side 2 to Side 1		0.4 x VCC2 to 0.9 V		67	109	ns
$PWD_{2\text{-}1}$ (1)	Pulse Width Distortion $\lvert t_{pHL2\text{-}1} - t_{pLH2\text{-}1}\rvert$				20	49	ns
t_{LOOP1} (1)	Round-trip propagation delay on Side 1	See Figure 2; R_1 = 953 Ω, C_1 = 40 pF R_2 = 95.3 Ω, C_2 = 400 pF	0.4 V to 0.3 x VCC1		100	165	ns
4.5V ≤ VCC1, VCC2 ≤ 5.5V							
t_{f1}	Output Signal Fall Time (SDA1, SCL1)	See Figure 1 R_1 = 1430 Ω, C_1 = 40 pF	0.7 x VCC1 to 0.3 x VCC1	6	11	20	ns
			0.9 x VCC1 to 900 mV	13	21	39	
t_{f2}	Output Signal Fall Time (SDA2, SCL2)	See Figure 1 R_2 = 143 Ω, C_2 = 400 pF	0.7 x VCC2 to 0.3 x VCC2	10	18	35	ns
			0.9 x VCC2 to 400 mV	28	41	76	
$t_{pLH1\text{-}2}$	Low-to-High Propagation Delay, Side 1 to Side 2	See Figure 1 R_1 = 1430 Ω, R_2 = 143 Ω, $C_{1,\,2}$ = 10 pF	0.55 V to 0.7 x VCC2		31	62	ns
$t_{PHL1\text{-}2}$	High-to-Low Propagation Delay, Side 1 to Side 2		0.7 V to 0.4 V		70	139	ns
$PWD_{1\text{-}2}$	Pulse Width Distortion $\lvert t_{pHL1\text{-}2} - t_{pLH1\text{-}2}\rvert$				38	80	ns
$t_{PLH2\text{-}1}$ (1)	Low-to-High Propagation Delay, Side 2 to Side 1		0.4 x VCC2 to 0.7 x VCC1		55	80	ns
$t_{PHL2\text{-}1}$ (1)	High-to-Low Propagation Delay, Side 2 to Side 1		0.4 x VCC2 to 0.9 V		47	85	ns
$PWD_{2\text{-}1}$ (1)	Pulse Width Distortion $\lvert t_{pHL2\text{-}1} - t_{pLH2\text{-}1}\rvert$				8	21	ns
t_{LOOP1} (1)	Round-trip propagation delay on Side 1	See Figure 2; R_1 = 1430 Ω, C1 = 40 pF R_2 = 143 Ω, C2 = 400 pF	0.4 V to 0.3 x VCC1		110	180	ns

(1) This parameter does not apply to the ISO1541 SCL1 line as it is uni-directional.

TIMING CHARACTERISTICS

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{SP}	Input Noise Filter		5	12		ns
t_{UVLO}	Time to recover from *Undervoltage Lock-out*	See Figure 4 2.7 V to 0.9 V	30	50	110	µs

PARAMETER MEASUREMENT INFORMATION

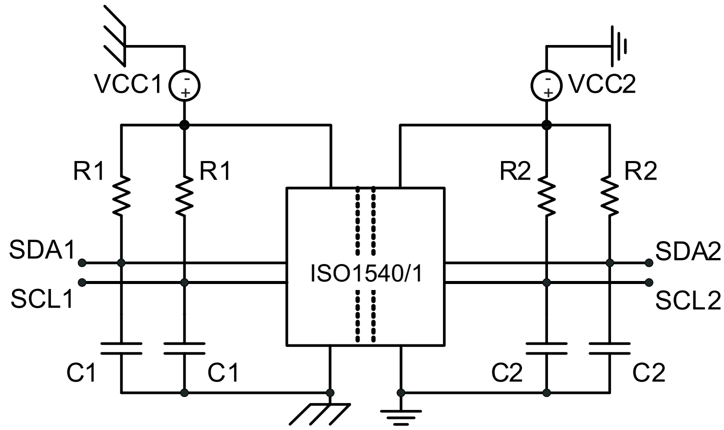


Figure 1. Test Diagram

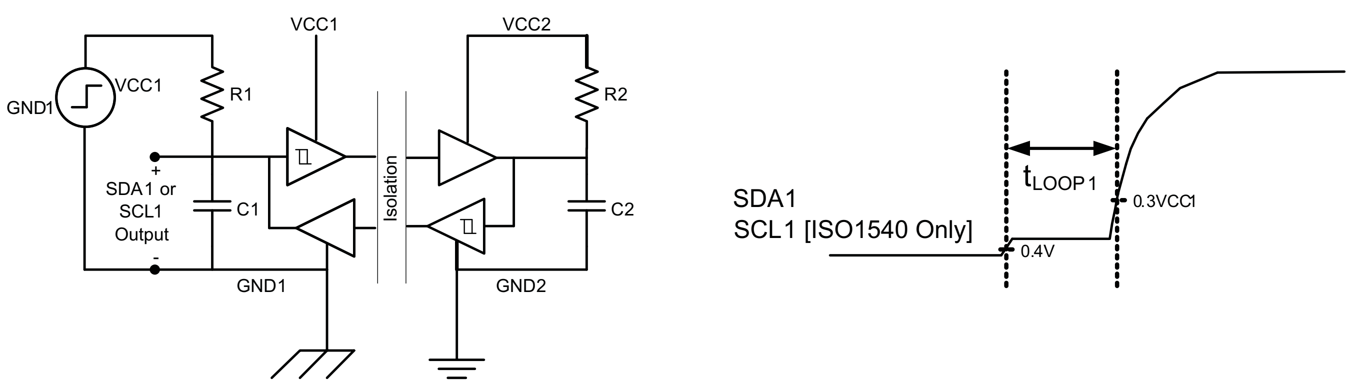


Figure 2. t_{Loop1} Setup and Timing Diagram

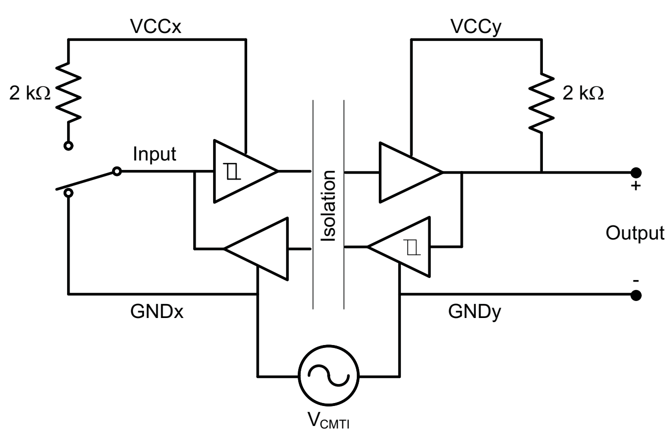
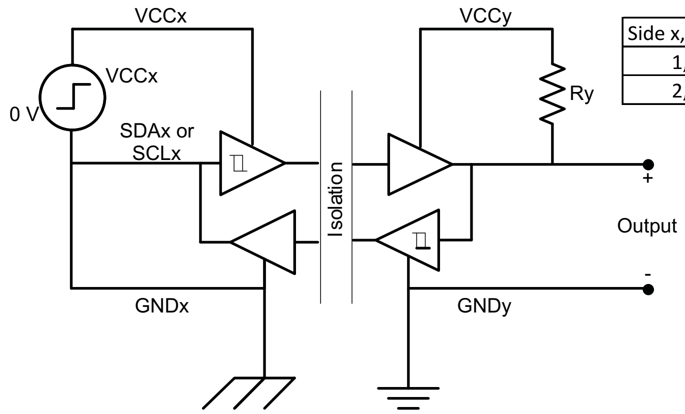


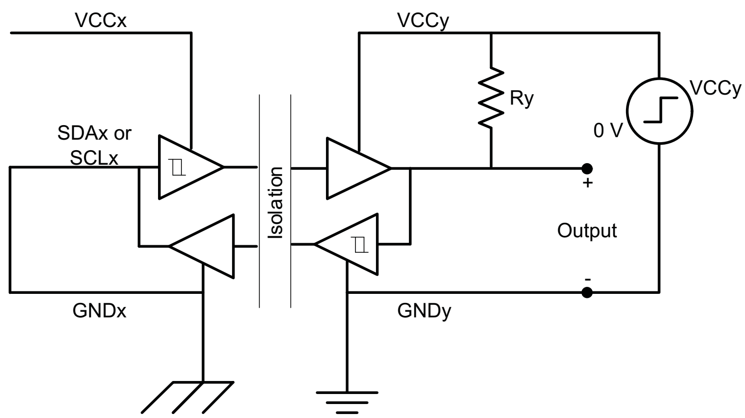
Figure 3. Common-Mode Transient Immunity Test Circuit

PARAMETER MEASUREMENT INFORMATION (continued)



Side x, Side y	Vccx, Vccy	Ry
1, 2	3.3V, 3.3V	95.3Ω
2, 1	3.3V, 3.3V	953Ω

or



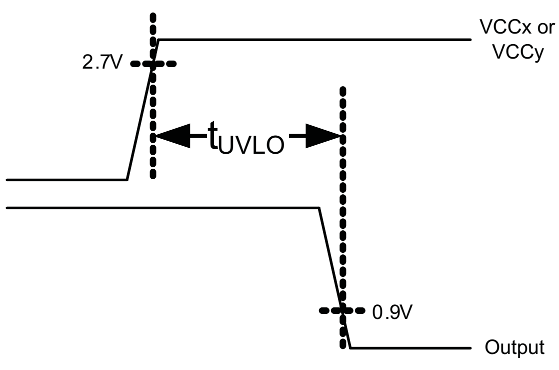


Figure 4. t_{UVLO} Test Circuit and Timing Diagrams

DEVICE INFORMATION

Table 2. IEC INSULATION AND SAFETY-RELATED SPECIFICATION FOR D-8 PACKAGE
Over recommended operating conditions, unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
L(I01)	Minimum air gap (Clearance)	Shortest terminal-to-terminal distance through air	4.8			mm
L(I02)	Minimum external tracking (Creepage)	Shortest terminal-to-terminal distance across the package surface	4.3			mm
CTI	Tracking resistance (comparative tracking index)	DIN IEC 60112 / VDE 0303 Part 1	>400			V
	Minimum internal gap (internal clearance)	Distance through the insulation	0.014			mm
R_{IO}	Isolation resistance, input to output (1)	V_{IO} = 500 V, T_A < 100°C		$>10^{12}$		Ω
		V_{IO} = 500 V, 100°C ≤ T_A		$>10^{11}$		Ω
C_{IO}	Barrier capacitance, input to output (1)	V_{IO} = 0.4 x sin(2E6πt)		1		pF
C_I	Input capacitance (2)		See Electrical Characteristics			pF

(1) All pins on each side of the barrier tied together creating a two-terminal device.
(2) Measured from input pin to ground.

NOTE

Creepage and clearance requirements should be applied according to the specific application isolation standards. Care should be taken to maintain these distances on a board design to ensure that the mounting pads for the isolator do not reduce this distance.

Creepage and clearance on the printed-circuit board become equal in certain cases. Techniques such as inserting grooves and/or ribs on the printed circuit board are used to help increase these specifications.

Table 3. IEC 60747-5-2 INSULATION CHARACTERISTICS (1)
Over recommended operating conditions, unless otherwise noted

PARAMETER		TEST CONDITIONS	SPECIFICATION	UNIT
V_{IORM}	Maximum working insulation voltage		566	V_{PEAK}
V_{PR}	Input-to-Output test voltage per IEC 60747-5-2	Method a, After environmental tests subgroup 1, $V_{PR} = V_{IORM}$ x 1.6, t = 10 sec, Partial Discharge < 5 pC	906	
		Method b1, After environmental tests subgroup 1, $V_{PR} = V_{IORM}$ x 1.875, t = 1 sec (100% production), Partial Discharge < 5 pC	1062	
		After Input/Output safety test subgroup 2/3, $V_{PR} = V_{IORM}$ x 1.2, t = 10 sec, Partial Discharge < 5 pC	680	
V_{IOTM}	Transient overvoltage per IEC 60747-5-2	$V_{TEST} = V_{OITM}$ t = 60 sec (qualification) t = 1 sec (100% production)	4000	
R_S	Insulation resistance	V_{IO} = 500 V at T_S	$>10^9$	Ω
	Pollution degree		2	

(1) Climatic Classification 40/125/21

Table 4. IEC 60664-1 RATINGS TABLE

PARAMETER	TEST CONDITIONS	SPECIFICATION
Basic isolation group	Material group	II
Installation classification	Rated mains voltage ≤ 150 V_{RMS}	I–IV
	Rated mains voltage ≤ 300 V_{RMS}	I–III
	Rated mains voltage ≤ 400 V_{RMS}	I–II

Table 5. REGULATORY INFORMATION

VDE	CSA	UL
Certified according to DIN EN 60747-5-2 (VDE 0884 Part 2) and EN 61010-1	Approved under CSA Component Acceptance Notice #5A, CSA/IEC 60950-1 & CSA/IEC 61010-1	Recognized under UL 1577 Component Recognition Program
Basic Insulation Maximum Transient Overvoltage, 4000 V_{PK} Maximum Surge Voltage, 4000 V_{PK} Maximum Working Voltage, 566 V_{PK}	Basic insulation per CSA 60950-1-07 and IEC 60950-1 (2nd Ed), 390 V_{RMS} maximum working voltage Basic insulation per CSA 61010-1-04 and IEC 61010-1 (2nd Ed), 300 V_{RMS} maximum working voltage Reinforced insulation per CSA 61010-1-04 and IEC 61010-1 (2nd Ed), 150 V_{RMS} maximum working voltage	Single Protection Isolation Voltage, 2500 V_{RMS} (1)
File number: 40016131 (pending)	File number: 220991 (pending)	File number: E181974

(1) Production tested ≥ 3000 V_{RMS} for 1 second in accordance with UL 1577.

IEC SAFETY LIMITING VALUES

Safety limiting intends to prevent potential damage to the isolation barrier upon failure of input or output circuitry. A failure of the IO can allow low resistance to ground or the supply and, without current limiting, dissipate sufficient power to overheat the die and damage the isolation barrier potentially leading to secondary system failures.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_S	Safety input, output, or supply current	D-8	θ_{JA} = 114.6°C/W, V_I = 5.5V, T_J = 150°C, T_A = 25°C			198	mA
			θ_{JA} = 114.6°C/W, V_I = 3.6V, T_J = 150°C, T_A = 25°C			303	
T_S	Maximum case temperature					150	°C

The safety-limiting constraint is the absolute maximum junction temperature specified in the absolute maximum ratings table. The power dissipation and junction-to-air thermal impedance of the device installed in the application hardware determines the junction temperature. The assumed junction-to-air thermal resistance in the *Thermal Information* table is that of a device installed on a High-K Test Board for Leaded Surface Mount Packages. The power is the recommended maximum input voltage times the current. The junction temperature is then the ambient temperature plus the power times the junction-to-air thermal resistance.

ISO154x THERMAL DERATING

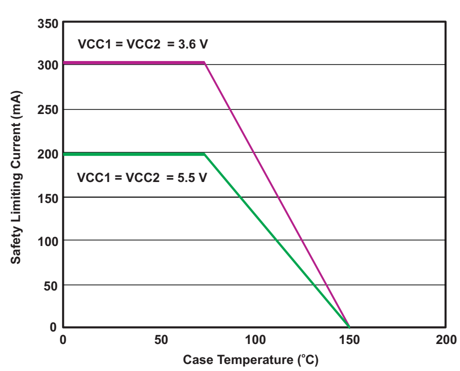


Figure 5.

APPLICATION INFORMATION

I²C™ Bus Overview

The I²C (Inter-Integrated Circuit) bus is a single-ended, multi-master, 2-wire bus for efficient inter-IC communication in half-duplex mode.

I²C uses open-drain technology, requiring two lines, Serial Data (SDA) and Serial Clock (SCL), to be connected to VDD by resistors (see Figure 6). Pulling the line to ground is considered a logic Zero while letting the line float is a logic One. This is used as a channel access method. Transitions of logic states must occur while SCL is Low, transitions while SCL is high indicate START and STOP conditions. Typical supply voltages are 3.3 V and 5 V, although systems with higher or lower voltages are permitted.

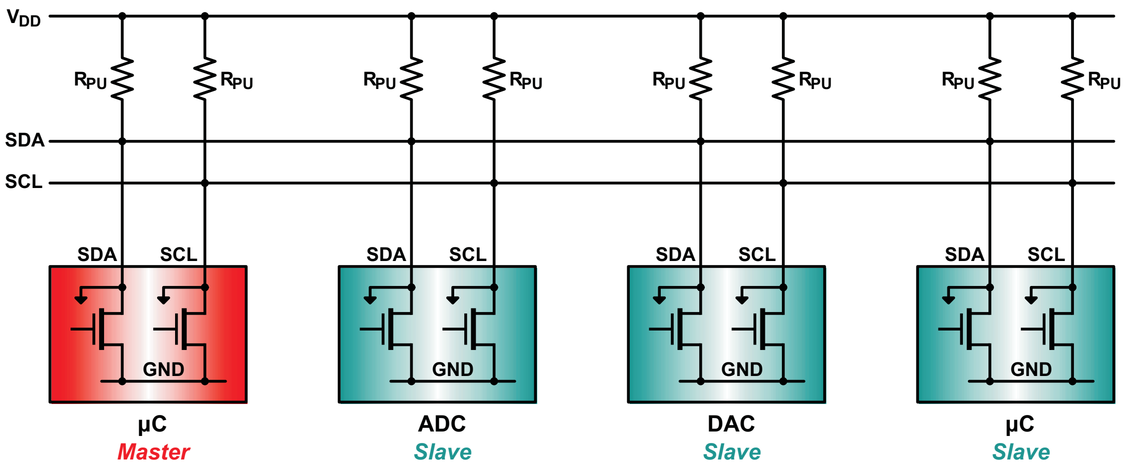


Figure 6. I²C BUS

I²C communication uses a 7-bit address space with 16 reserved addresses, so a theoretical maximum of 112 nodes can communicate on the same bus. In praxis, however, the number of nodes is limited by the specified, total bus capacitance of 400 pF, which restricts communication distances to a few meters.

The specified signaling rates for the ISO1540 and ISO1541 are 100 kbps (Standard mode), 400 kbps (Fast mode), 1 Mbps (Fast mode plus).

The bus has two roles for nodes: master and slave. A master node issues the clock, slave addresses, and also initiates and ends data transactions. A slave node receives the clock and addresses and responds to requests from the master. Figure 7 shows a typical data transfer between master and slave.

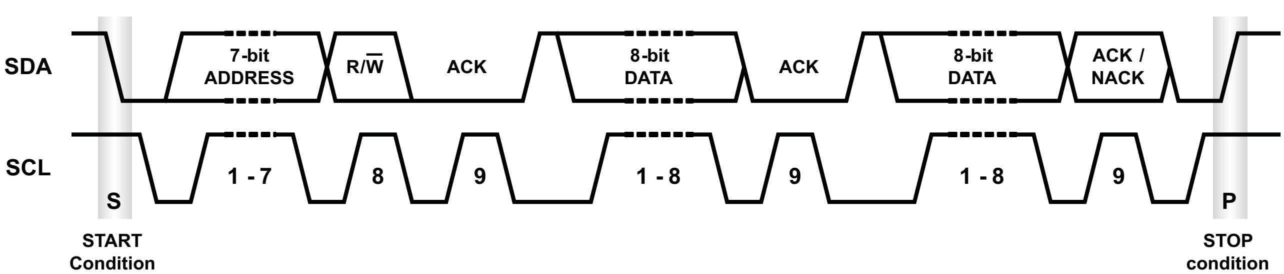


Figure 7. Timing Diagram of a Complete Data Transfer

The master initiates a transaction by creating a START condition, following by the 7-bit address of the slave it wishes to communicate with. This is followed by a single Read/Write bit, representing whether the master wishes to write to (0), or to read from (1) the slave. The master then releases the SDA line to allow the slave to acknowledge the receipt of data.

The slave responds with an acknowledge bit (ACK) by pulling SDA low during the entire high time of the 9th clock pulse on SCL, after which the master continues in either transmit or receive mode (according to the R/W bit sent), while the slave continues in the complementary mode (receive or transmit, respectively).

The address and the 8-bit data bytes are sent most significant bit (MSB) first. The START bit is indicated by a high-to-low transition of SDA while SCL is high. The STOP condition is created by a low-to-high transition of SDA while SCL is high.

If the master writes to a slave, it repeatedly sends a byte with the slave sending an ACK bit. In this case, the master is in master-transmit mode and the slave is in slave-receive mode.

If the master reads from a slave, it repeatedly receives a byte from the slave, while acknowledging (ACK) the receipt of every byte but the last one (see Figure 8). In this situation the master is in master-receive mode and the slave is in slave-transmit mode.

The master ends the transmission with a STOP bit, or may send another START bit to maintain bus control for further transfers.

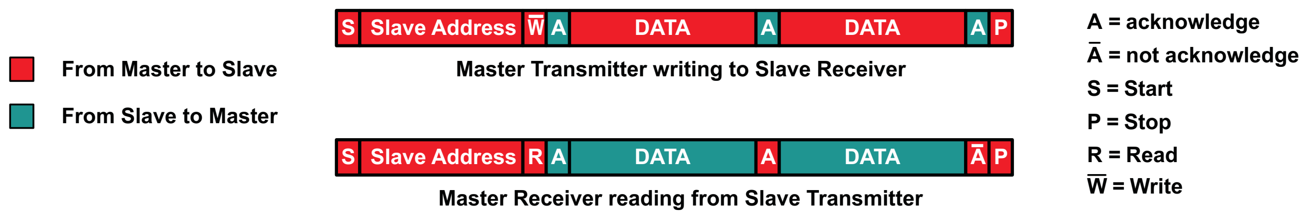


Figure 8. Transmit or Receive Mode Changes During a Data Transfer

When writing to a slave, a master mainly operates in transmit-mode and only changes to receive-mode when receiving acknowledgment from the slave.

When reading from a slave, the master starts in transmit-mode and then changes to receive-mode after sending a READ request (R/W bit = 1) to the slave. The slave continues in the complementary mode until the end of a transaction.

Note, that the master ends a reading sequence by not acknowledging (NACK) the last byte received. This procedure resets the slave state machine and allows the master to send the STOP command.

Isolator Functional Principle

To isolate a bidirectional signal path (SDA or SCL), the ISO1540 internally splits a bidirectional line into two unidirectional signal lines, each of which is isolated via a single-channel digital isolator. Each channel output is made open-drain to comply with the open-drain technology of I^2C. Side 1 of the ISO1540 connects to a low-capacitance I^2C node, while Side 2 is designed for connecting to a fully loaded I^2C bus with up to 400 pF capacitance.

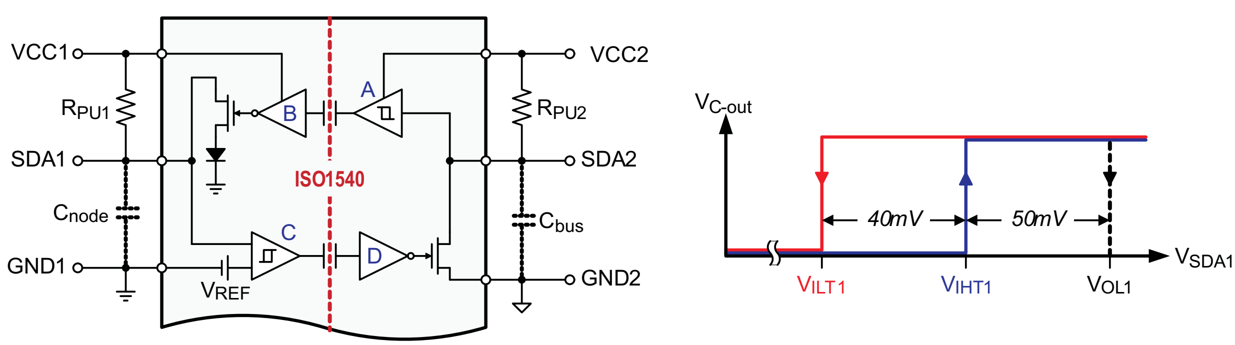


Figure 9. SDA Channel Design and Voltage Levels at SDA1

At first sight, the arrangement of the internal buffers suggests a closed signal loop that is prone to latch-up. However, this loop is broken by implementing an output buffer (B) whose output low-level is raised by a diode drop to approximately 0.75 V, and the input buffer (C) that consists of a comparator with defined hysteresis. The comparator's upper and lower input thresholds then distinguish between the proper low-potential of 0.4 V maximum driven directly by SDA1 and the buffered output low-level of B.

Figure 10 demonstrate the switching behavior of the I^2C isolator, ISO1540, between a master node at SDA1 and a heavy loaded bus at SDA2

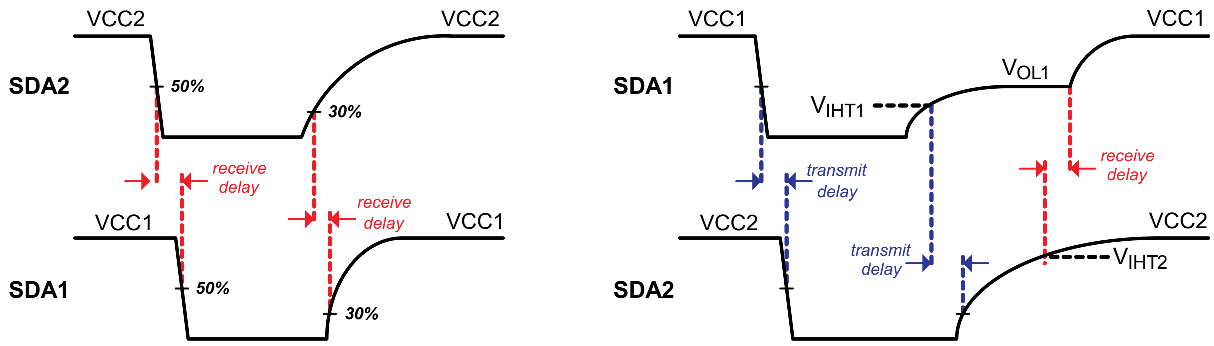


Figure 10. SDA Channel Timing in Receive and Transmit Directions

Receive Direction (left diagram)

When the I^2C bus drives SDA2 low, SDA1 follows after a certain delay in the receive path. Its output low will be the buffered output of V_{OL1} = 0.75 V, which is sufficiently low to be detected by Schmitt-trigger inputs with a minimum input-low voltage of V_{IL} = 0.9 V at 3 V supply levels.

Once SDA2 is released, its voltage potential increases towards VCC2 following the time-constant formed by R_{PU2} and C_{bus}. After the receive delay, SDA1 is released and also rises towards VCC1, following the time-constant R_{PU1} x C_{node}. Because of the significant lower time-constant, SDA1 may reach VCC1 before SDA2 reaches VCC2 potential.

Transmit Direction (right diagram)

When a master drives SDA1 low, SDA2 follows after a certain delay in the transmit direction. When SDA2 turns low it also causes the output of buffer B to turn low but at a higher 0.75 V level. This level cannot be observed immediately as it is overwritten by the master's lower low-level.

However, when the master releases SDA1, its voltage potential increases and first must pass the upper input threshold of the comparator, V_{IHT1}, to release SDA2. SDA1 then increases further until it reaches the buffered output level of V_{OL1} = 0.75 V, maintained by the receive path. Once comparator C turns high, SDA2 is released after the delay in transmit direction. It takes another receive delay until B's output turns high and fully releases SDA1 to move towards VCC1 potential.

Typical Application Circuit

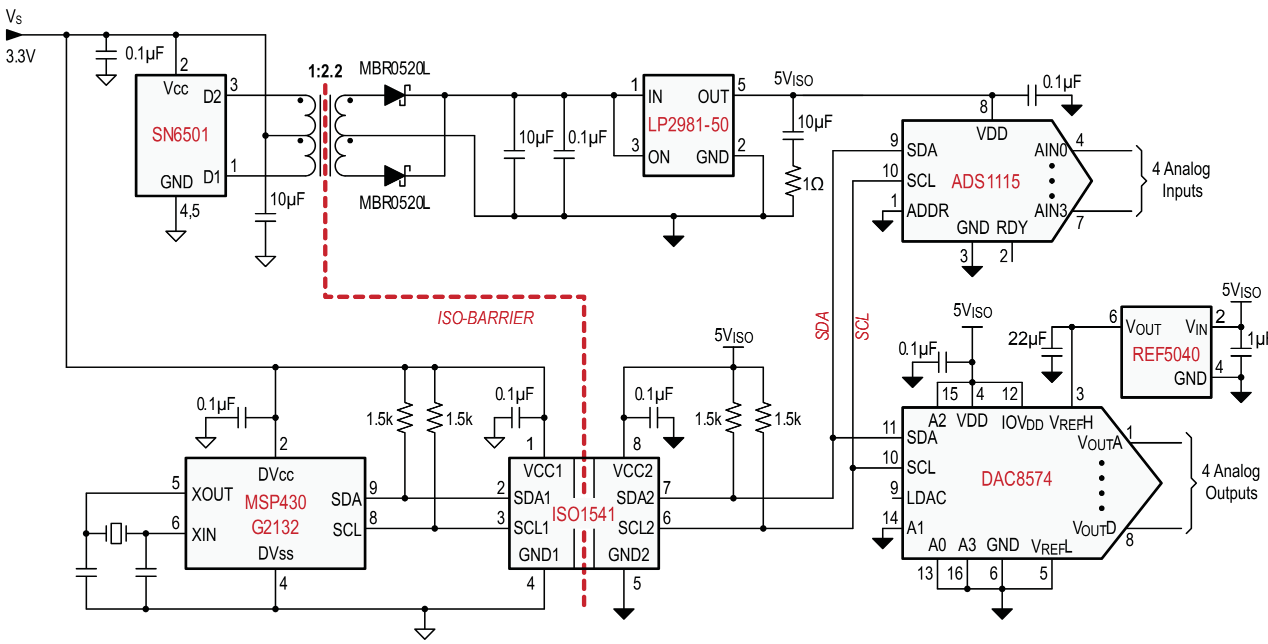


Figure 11. Isolated I²C Data Acquisition System

In Figure 11, the ultra low-power micro controller, MSP430G2132, controls the I²C data traffic of configuration data and conversion results for the analog inputs and outputs. Low-power data converters build the analog interface to sensors and actuators. The ISO1541 provides the necessary isolation between different ground potentials of the system controller, remote sensor, and actuator circuitry to prevent ground loop currents that otherwise may falsify the acquired data.

The entire circuit operates from a single 3.3 V supply. A low-power push-pull converter, SN6501, drives a center-tapped transformer whose output is rectified and linearly regulated to provide a stable 5 V supply for the data converters.

TYPICAL CHARACTERISTICS

SIDE 1 OUTPUT LOW VOLTAGE
vs FREE-AIR TEMPERATURE

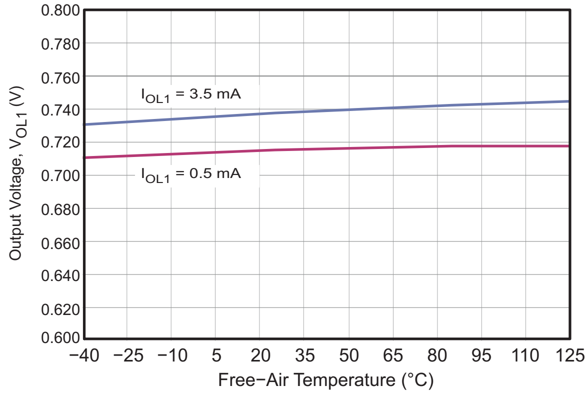


Figure 12.

SIDE 1 OUTPUT LOW CURRENT
vs S_{DA1} or S_{CL1} APPLIED VOLTAGE

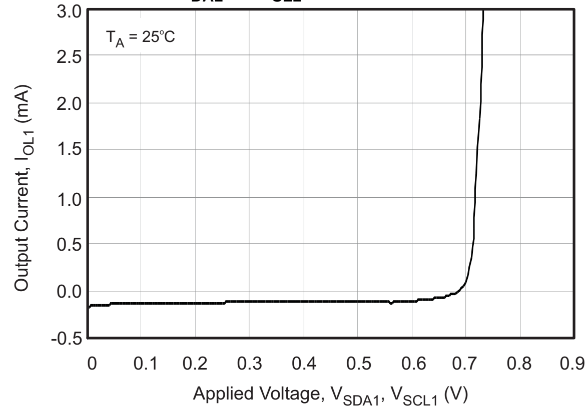


Figure 13.

SIDE 1 OUTPUT FALL TIME
vs FREE-AIR TEMPERATURE

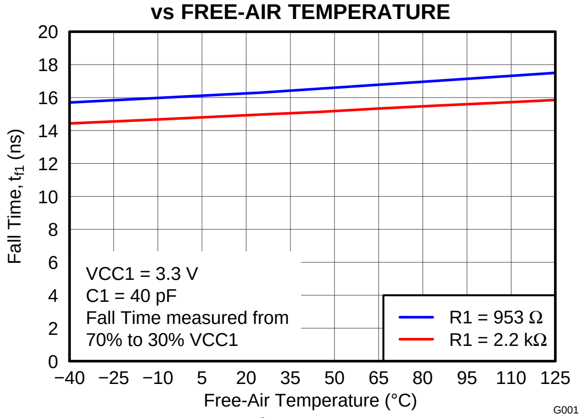


Figure 14.

SIDE 1 OUTPUT FALL TIME
vs FREE-AIR TEMPERATURE

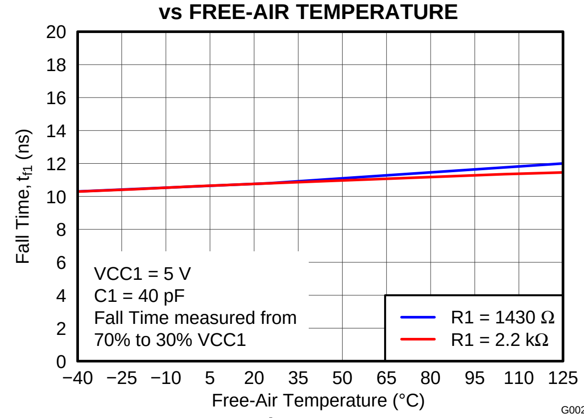


Figure 15.

SIDE 2 OUTPUT FALL TIME
vs FREE-AIR TEMPERATURE

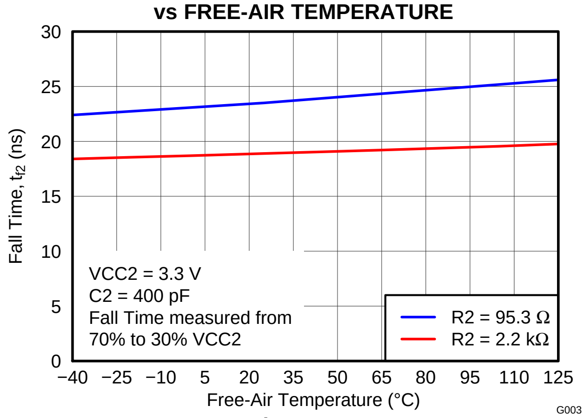


Figure 16.

SIDE 2 OUTPUT FALL TIME
vs FREE-AIR TEMPERATURE

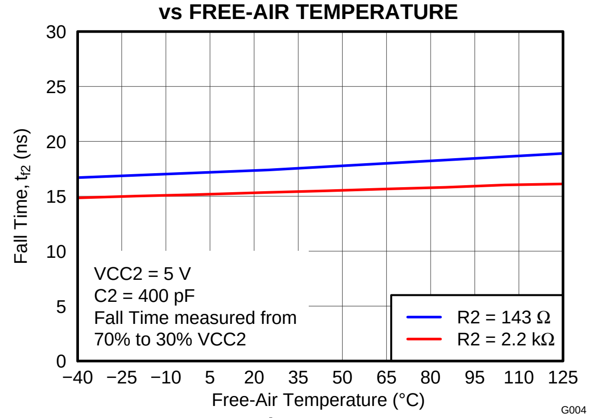


Figure 17.

TYPICAL CHARACTERISTICS (continued)

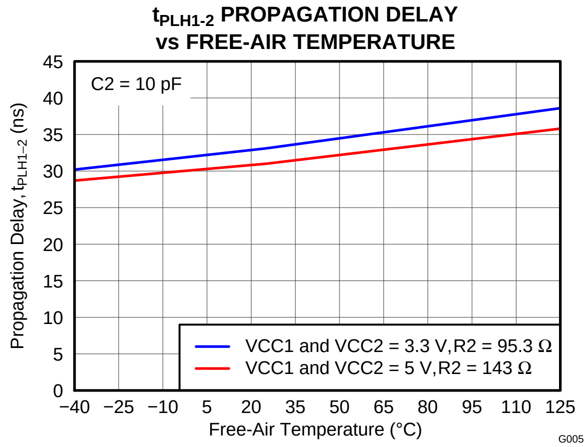


Figure 18.

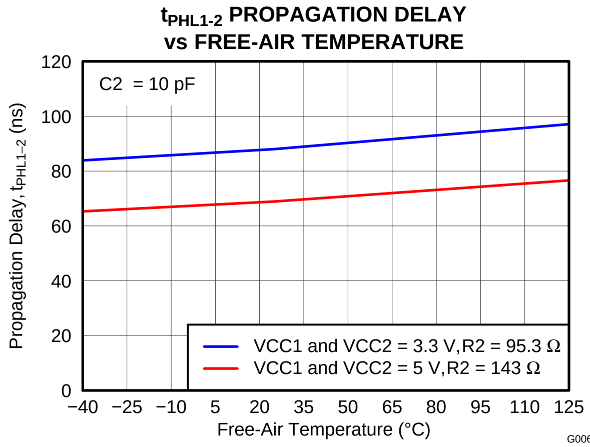


Figure 19.

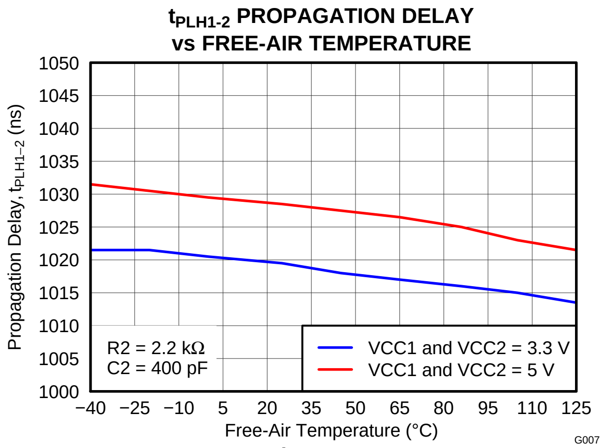


Figure 20.

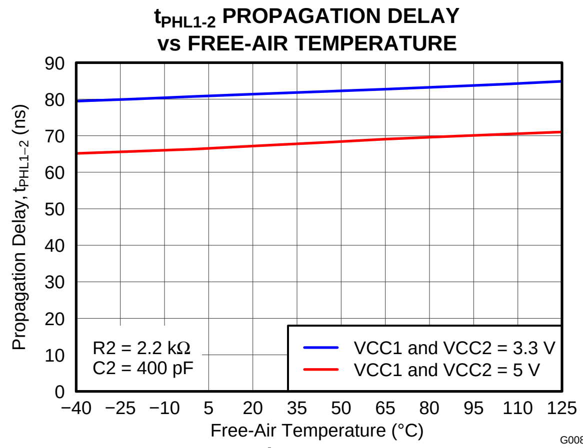


Figure 21.

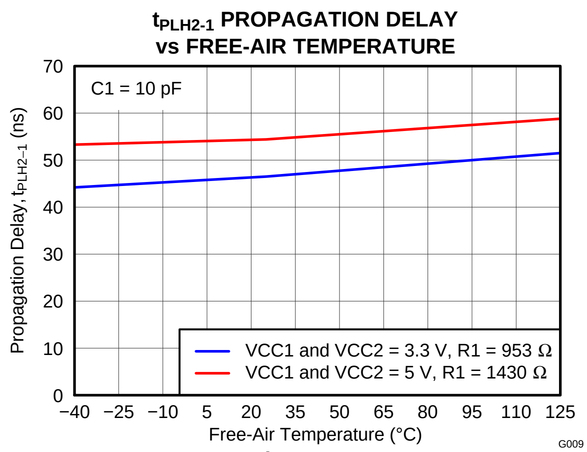


Figure 22.

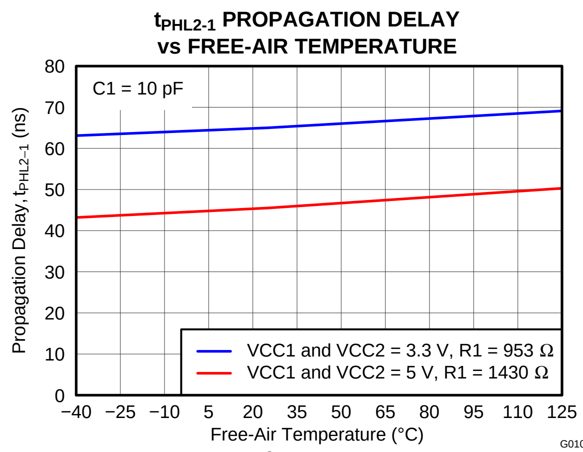


Figure 23.

TYPICAL CHARACTERISTICS (continued)

t_{PLH2-1} PROPAGATION DELAY vs FREE-AIR TEMPERATURE

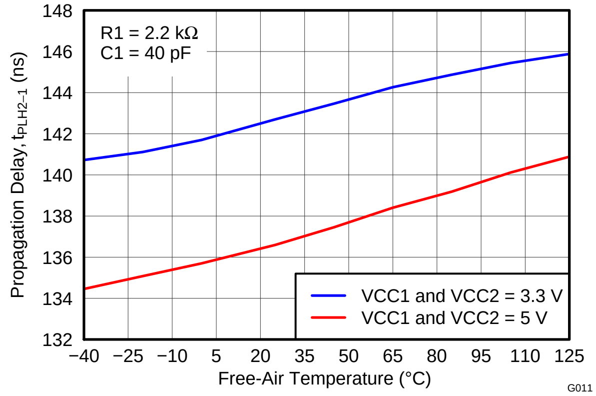


Figure 24.

t_{PHL2-1} PROPAGATION DELAY vs FREE-AIR TEMPERATURE

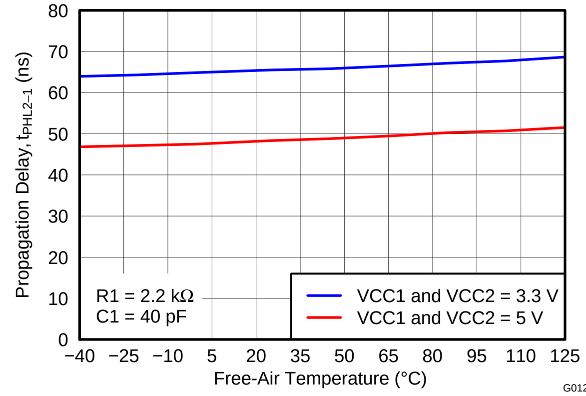


Figure 25.

t_{LOOP1} vs FREE-AIR TEMPERATURE

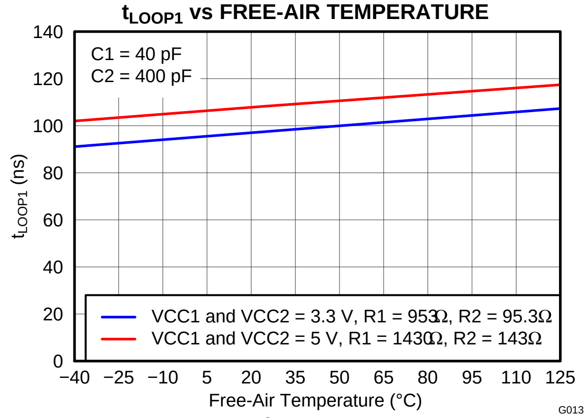


Figure 26.

t_{LOOP1} vs FREE-AIR TEMPERATURE

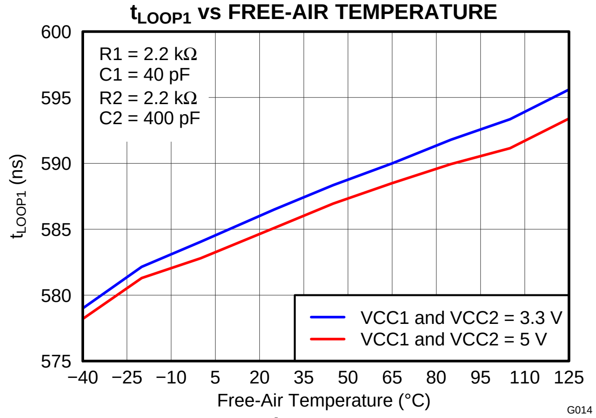


Figure 27.

CMTI vs FREE-AIR TEMPERATURE

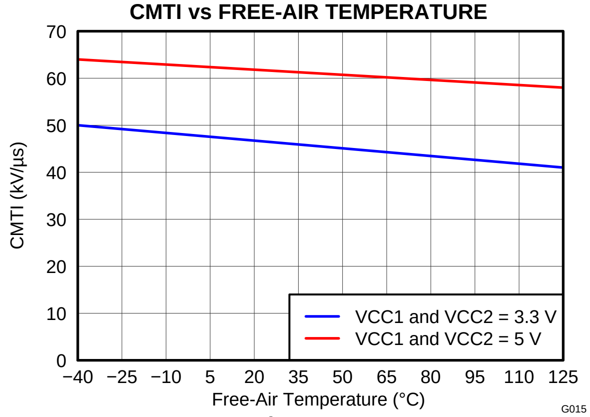


Figure 28.

TYPICAL CHARACTERISTICS (continued)

SIDE 1 LOW-TO-HIGH TRANSITION

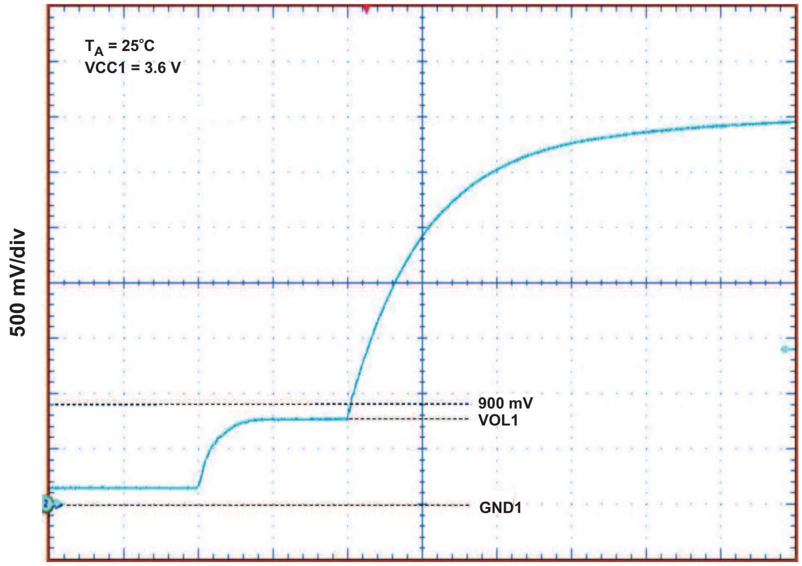


Figure 29.

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/ Ball Finish	MSL Peak Temp [3]	Samples (Requires Login)
ISO1540D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
ISO1540DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
ISO1541D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
ISO1541DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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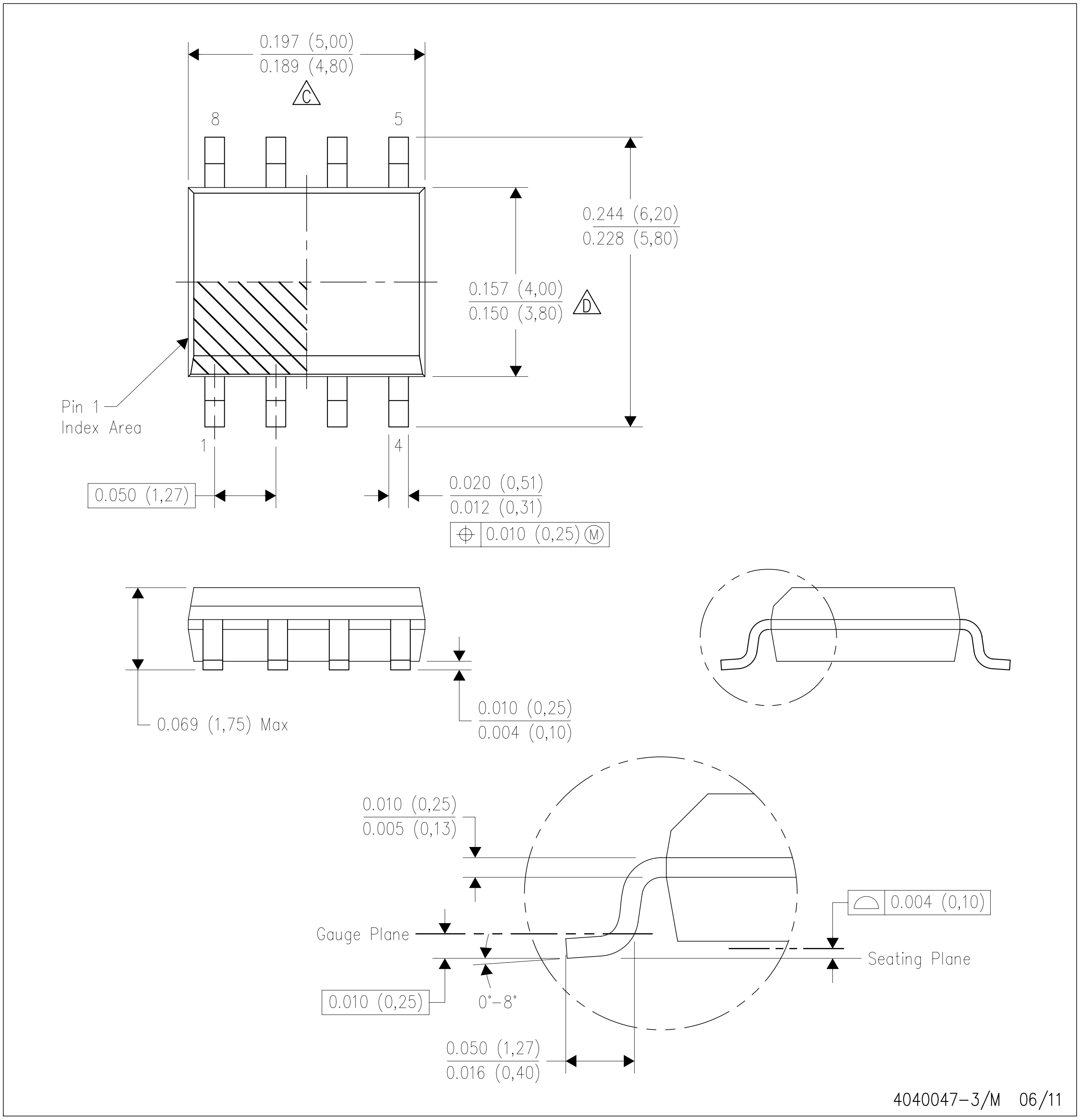
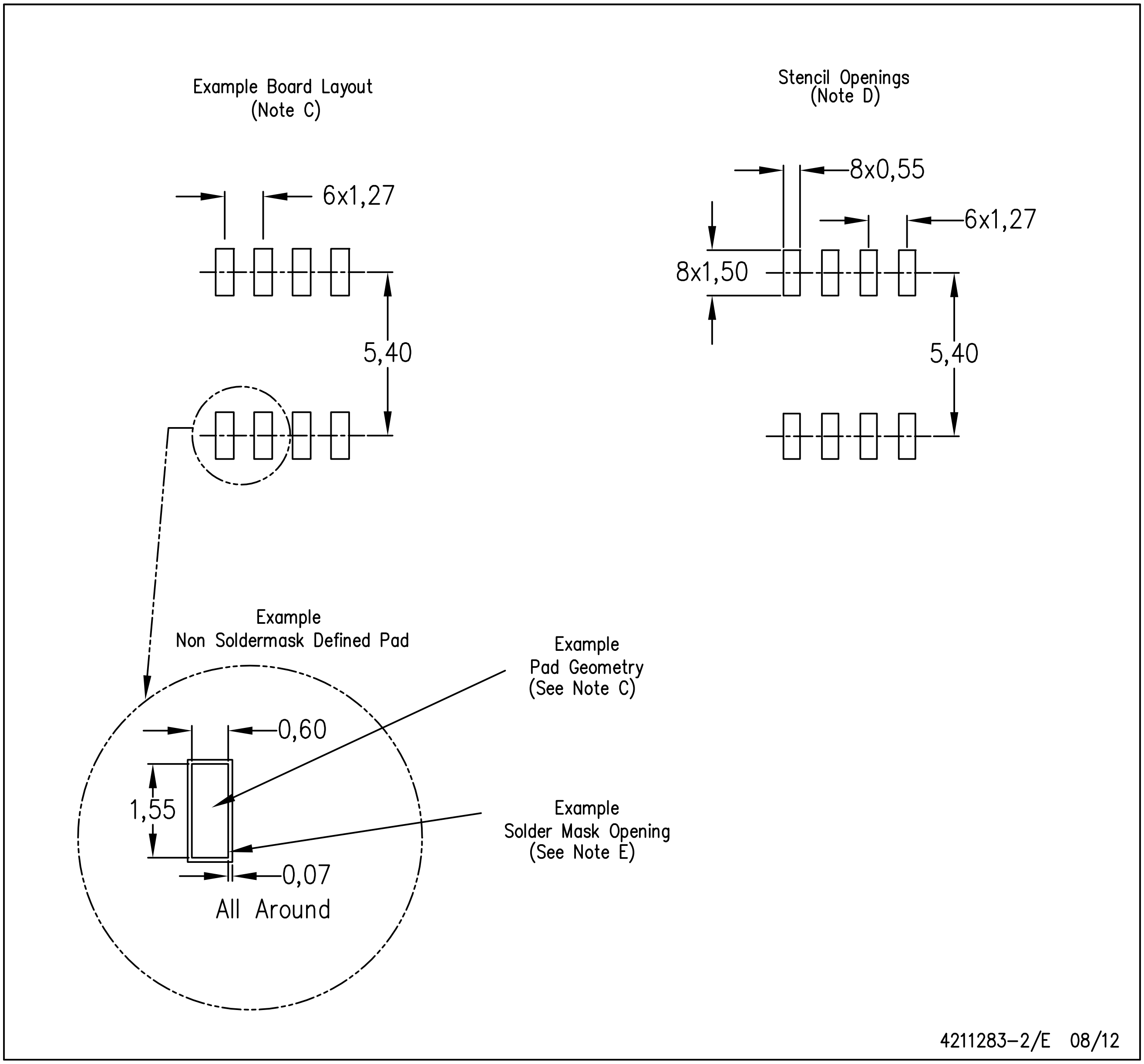
D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS-012 variation AA.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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